PATENT ABSTRACTS OF JAPAN

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(21)Application number : 03-269075
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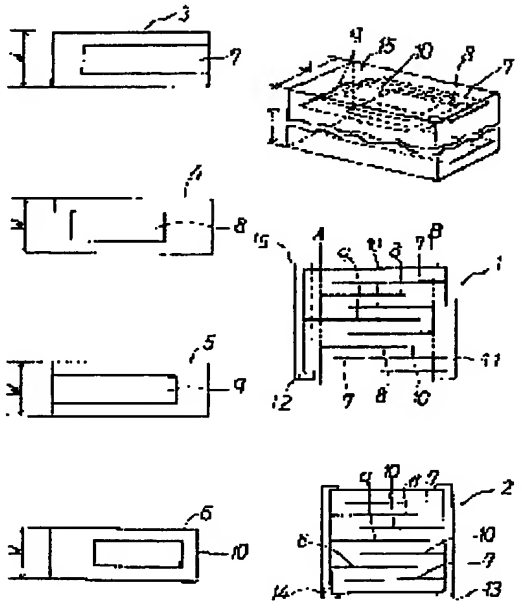
(71)Applicant : TOKIN CORP
(72)Inventor : ABE MASATSUGU

(54) MANUFACTURE OF LAMINATED CERAMIC CAPACITOR

(57)Abstract:
PURPOSE: To easily adjust the rated voltage and the capacity of the title capacitor by a method wherein internal electrodes whose pattern is different are piled up regularly, ceramics and the internal electrodes in parts where internal electrode patterns are extracted to the surface of a chip before an outer electrode is formed are removed by using a grinding machine, a sandblast or the like.
CONSTITUTION: Individual ceramic dielectric layers, i.e., a ceramic dielectric layer 3 in which an internal electrode 7 protrudes to the right-side end part, a ceramic dielectric layer 4 in which an internal electrode 8 is put aside to the left-side end part, a ceramic dielectric layer 5 in which an internal electrode 9 protrudes to the left-side end part and a ceramic dielectric layer 6 in which an internal electrode 10 is put aside to the right-side end part, are laminated; a laminated body 15 is formed. The laminated body 15 is ground up to parts A, B by using a grinding machine, a sandblast or the like; all the internal electrodes 7, 8, 9, 10 are taken out and used as electrodes; outer electrodes 13, 14 are formed. Thereby, the rated voltage and the capacity of the title capacitor can be changed, the thickness of the laminated body can be reduced, the rated voltage is reduced and the electrostatic capacity of the title capacitor can be changed largely.



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	4/34		8019－5Ｅ		

審査請求　未請求　請求項の数１(全　４　頁)

(21)出願番号　特願平3－269075

(22)出願日　平成３年(1991)９月19日

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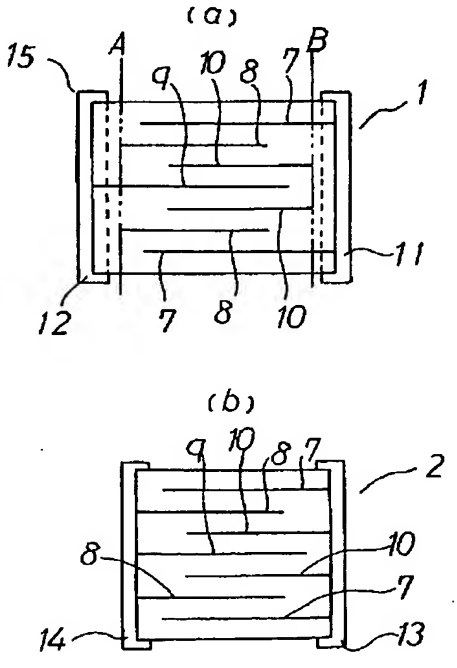
(54)【発明の名称】　積層セラミックコンデンサーの製造方法

(57)【要約】

【目的】　距離及び容量の異なる複数の内部電極を有し、複数層の内部電極が複数層の誘電体層を積層する所定の積層セラミックコンデンサーの厚さを小さくし、定格電圧を小さくし、静電容量は倍以上になる積層セラミックコンデンサーを提供すること。

【構成】　内部電極Ａ７，Ｂ８，Ｃ９，Ｄ１０と外部電極$A_1$１１，$A_2$１２とを有するセラミック誘電体Ａ３，Ｂ４，Ｃ５，Ｄ６のセラミック誘電体層を積層して積層体１５を形成し、この積層体１５をＡ，Ｂまで研削して、内部電極Ａ７，Ｂ８，Ｃ９，Ｄ１０を全て取出し、電極として外部電極$B_1$１３，$B_2$１４を形成する積層セラミックコンデンサーである。



【特許請求の範囲】
【請求項１】　複数層の内部電極を有する複数層の誘電体層を積層する積層セラミックコンデンサーにおいて、距離及び容量の異なる複数の内部電極を規則的に積層しておき、外部電極を形成する前に研削機やサンドブラスト等を用い、積層セラミックコンデンサーの内部電極の直角方向の長手の端面のセラミック及び内部電極を削除することによって、内部電極を端面に取出し外部電極につなぎ、誘電体層の距離及び容量を形成する有効層数を変えることで定格電圧・容量を調整変化することを特徴とする積層セラミックコンデンサーの製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、積層セラミックコンデンサーの製造方法に関するものである。
【０００２】
【従来の技術】従来この種の積層セラミックコンデンサーは、例えばキャリアフィルム等に均一な厚みで成膜し、同一パターンを印刷・積み重ねるために定格電圧の調整ができない。また、容量に関しても一度所定枚数重ねると容量が決ってしまうため、容量を調整することができないというような欠点があった。
【０００３】
【発明が解決しようとする課題】本発明は、これらの欠点を除去するためキャリアフィルムに均一な厚みを成膜し、キャリアフィルムに印刷成膜した後、内部電極パターンの異なるものを印刷し、そのパターンの異なる内部電極を規則正しく積み重ね、外部電極を形成する前に内部電極パターンがチップ表面に取出された部分を研削機やサンドブラスト等を用い、セラミック及び内部電極を削除することによって、定格電圧・容量を調整する積層セラミックコンデンサーを提供することを目的とする。
【０００４】
【課題を解決するための手段】本発明は、複数層の内部電極を有する複数層の誘電体層を積層する積層セラミックコンデンサーにおいて、距離及び容量の異なる複数の内部電極を規則的に積層しておき、外部電極を形成する前に研削機やサンドブラスト等を用い、積層セラミックコンデンサーの内部電極の直角方向の長手の端面のセラミック及び内部電極を削除することによって、内部電極を端面に取出し外部電極につなぎ誘電体層の距離及び容量を形成する有効層数を変えることで定格電圧・容量を調整変化することを特徴とする積層セラミックコンデンサーの製造方法である。
【０００５】
【作用】本発明は、外部電極を形成する前に積層体の内部に挟んだ内部電極の一部がチップ表面に取出されている部分から研削機やサンドブラスト等を用いてセラミックや内部電極を削除することによって、定格電圧・容量を変更でき、積層体の厚みを小さくし、定格電圧も小さくなり、静電容量が２倍以上にできる積層セラミックコンデンサーが提供できる。
【０００６】
【実施例】実施例を以下に説明する。図１は、内部電極Ａ７が右側端部へでた幅Wのセラミック誘電体層Ａ３の平面図。図２は、内部電極Ｂ８が左側端部へよった幅Wのセラミック誘電体層Ｂ４の平面図。図３、は内部電極Ｃ９が左側端部へでた幅Wのセラミック誘電体層Ｃ５の平面図。図４は、内部電極Ｄ１０が右側端部へよった幅Wのセラミック誘電体層Ｄ６の平面図。図５は、図１・図２・図４・図３・図４・図２・図１のセラミック誘電体Ａ３、セラミック誘電体Ｂ４、セラミック誘電体Ｃ５、セラミック誘電体Ｄ６のセラミック誘電体層を積層して、積層体１５を形成した斜視図。図６の（ａ）は、図５の内部電極Ａ７，Ｂ８，Ｃ９，Ｄ１０を有する積層体１５に外部電極A_1，１１，A_2，１２を形成した積層セラミックコンデンサーＡ１の断面図。図６の（ｂ）は、ＡとＢまで研削し内部電極Ａ７，Ｂ８，Ｃ９，Ｄ１０を有し、外部電極B_1，１３，B_2，１４を施した積層セラミックコンデンサーＢ２の断面図。図７は、図６の積層セラミックコンデンサーＡ１の斜視図。図８は、図７の積層セラミックコンデンサーＢ２の斜視図。図７、図８に示すような積層セラミックコンデンサーＡ１・Ｂ２を製造する場合、図１・図２・図３・図４にそれぞれ示すセラミック誘電体層を、例えばセラミック誘電体層Ａ３→セラミック誘電体層Ｂ４→セラミック誘電体層Ｄ６→セラミック誘電体層Ｃ５→セラミック誘電体層Ｄ６→セラミック誘電体層Ｂ４→セラミック誘電体層Ａ３というように規則的に積層し、脱バインダー焼成工程を経ると図５に示すような幅W、厚さTの積層体１５が得られる。積層体１５の内部に形成されている内部電極Ａ７，内部電極Ｂ８，内部電極Ｃ９，内部電極Ｄ１０の内部電極の状態は、次のような特徴がある。図１のセラミック誘電体層Ａ３の一方表面上には内部電極Ａ７を形成させ、図２のセラミック誘電体層Ｂ４の一方表面上には内部電極Ｂ８が形成され、この内部電極は取出電極がない。図３のセラミック誘電体層Ｃ５の一方表面上には内部電極Ｃ９を形成させる。図４のセラミック誘電体層Ｄ６の一方表面上には内部電極Ｄ１０が形成され、この内部電極は取出電極がない。これらのセラミック誘電体層を例えば、セラミック誘電体層Ａ３→セラミック誘電体層Ｂ４→セラミック誘電体層Ｄ６→セラミック誘電体層Ｃ５→セラミック誘電体層Ｄ６→セラミック誘電体層Ｂ４→セラミック誘電体層Ａ３というように規則的に積層された時、図５に示すように積層体１５の寸法Wがセラミック誘電体層Ａ３・Ｂ４・Ｃ５・Ｄ６の幅方向Wと一致するようになり、かつ積層体１５の寸法Tが寸法Wより小さくなるように各セラミック誘電体層を例えば、セラミック誘電体層Ａ３→セラミック誘電体層Ｂ４→セラミック誘電体層Ｄ６→セラミック誘電体層Ｃ５→セラミック誘電体層

Ｄ６→セラミック誘電体層Ｂ４→セラミック誘電体層Ａ３の積層数が選ばれる。このように積層された場合、例えば図５の積層体１５内で内部電極Ａ７，Ｂ８，Ｃ９，Ｄ１０は水平方向に向いている。図５の積層体１５に対して、図７に示すように外部電極$A_1$１１，$A_2$１２が形成される。図７の積層体を幅方向の断面にしたものが図６の（ａ）である。図６の（ａ）のＡとＢの線まで研削機等の加工機でセラミックを研削して取除くと図６の（ｂ）のようになり、図６の（ｂ）に示すように、内部電極Ａ７，Ｂ８，Ｃ９，Ｄ１０を全て取出し電極として外部電極$B_1$１３，$B_2$１４を形成する。例えば、図５の積層体１５内でセラミック誘電体層Ｂ４・Ｄ６の電極がそれぞれ外部電極$A_1$１１，$A_2$１２形成して、表面に取出されるまで研削機やサンドブラスト等でセラミック及＊び内部電極を削除し、図８の外部電極$B_1$１３，$B_2$１４のように形成すると、図８に示すように図７の積層体の誘電層は１／３の厚みとなり、定格電圧は１／３ＷＶ、静電容量は約２．５倍に変えることが可能となる。更にセラミック誘電体に形成されるパターンを今回の４パターンから増やすことで、選択できる定格電圧、静電容量を多様化させることも可能である。又、今回の図５の積層体は水平方向に積層している例を示したが、垂直方向での作成も可能である。実際に試作を$Pb[(MgW)_{0.2}(NiNb)_{0.4}Ti_{0.4}]O_3$系の材料を用いて２０μｍ厚さのグリーンシートを使い、図７，図８のように積層体を作り、電気特性を測定したところ、表１のような結果が得られた。

【表１】

図番	定格電圧	研削機やｻﾝﾄﾞﾌﾞﾗｽﾄ等処理	静電容量（Ｃ値）	破壊電圧（Ｂ．Ｄ．Ｖ）
図７	７５Ｖ	無	０．４μＦ	１．０ＫＶ
図８	２５Ｖ	有	１　μＦ	３００Ｖ

【０００７】

【発明の効果】以上述べたごとく、本発明によれば内部に積層するパターンを多様化し、外部電極を形成する前に研削機やサンドブラスト等による外部電極取出し面を削除することによって、定格電圧、静電容量を変更することができるという利点を持った積層セラミックコンデンサーの提供が可能となった。

【図面の簡単な説明】

【図１】内部電極Ａ７が右側端部へでた幅Ｗのセラミック誘電体層Ａ３の平面図。

【図２】内部電極Ｂ８が左側端部へよった幅Ｗのセラミック誘電体層Ｂ４の平面図。

【図３】内部電極Ｃ９が左側端部へでた幅Ｗのセラミック誘電体層Ｃ５の平面図。

【図４】内部電極Ｄ１０が右側端部へよった幅Ｗのセラミック誘電体層Ｄ６の平面図。

【図５】図１・図２・図４・図３・図４・図２・図１のセラミック誘電体Ａ３、セラミック誘電体Ｂ４、セラミック誘電体Ｃ５、セラミック誘電体Ｄ６のセラミック誘電体層を積層して、積層体１５を形成した斜視図。

【図６】図６の（ａ）は、図５の内部電極Ａ７，Ｂ８，Ｃ９，Ｄ１０を有する積層体１５に外部電極A_1，A_2を形成した積層セラミックコンデンサーＡの断面図。図６の（ｂ）は、ＡとＢまで研削し内部電極Ａ７，Ｂ８，Ｃ９，Ｄ１０を有し、外部電極B_1，B_2を施した積層セラミックコンデンサーＢの断面図。

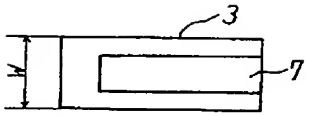
【図７】図６の（ａ）の積層セラミックコンデンサーＡの斜視図。

【図８】図６の（ｂ）の積層セラミックコンデンサーＢの斜視図。

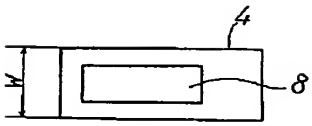
【符号の説明】

１　積層セラミックコンデンサーＡ
２　積層セラミックコンデンサーＢ
３　セラミック誘電体層Ａ
４　セラミック誘電体層Ｂ
５　セラミック誘電体層Ｃ
６　セラミック誘電体層Ｄ
７　内部電極Ａ
８　内部電極Ｂ
９　内部電極Ｃ
１０　内部電極Ｄ
１１　外部電極A_1
１２　外部電極A_2
１３　外部電極B_1
１４　外部電極B_2
１５　積層体

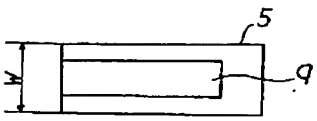
【図1】



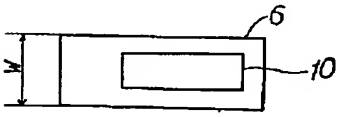
【図2】



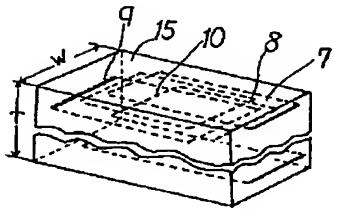
【図3】



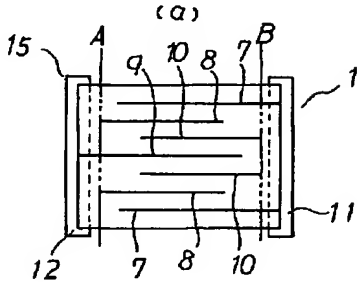
【図4】



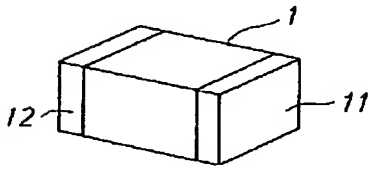
【図5】



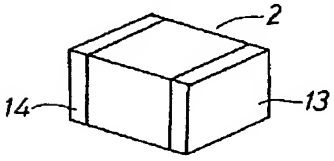
【図6】



【図7】



【図8】



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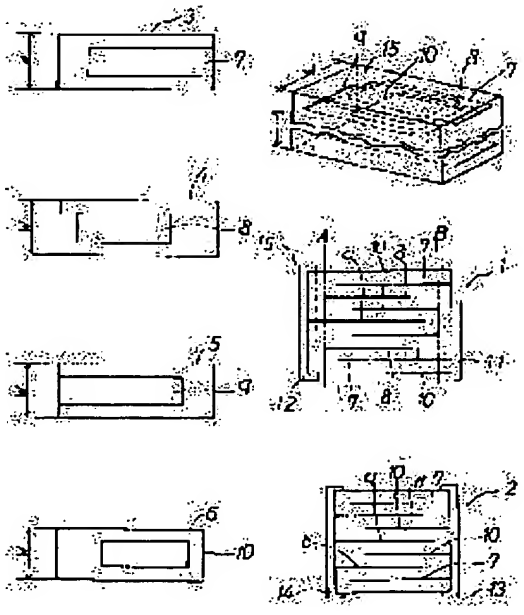
PURPOSE: To easily adjust the rated voltage and the capacity of the title capacitor by a method wherein internal electrodes whose pattern is different are piled up regularly, ceramics and the internal electrodes in parts where internal electrode patterns are extracted to the surface of a chip before an outer electrode is formed are removed by using a grinding machine, a sandblast or the like.
CONSTITUTION: Individual ceramic dielectric layers, i.e., a ceramic dielectric layer 3 in which an internal electrode 7 protrudes to the right-side end part, a ceramic dielectric layer 4 in which an internal electrode 8 is put aside to the left-side end part, a ceramic dielectric layer 5 in which an internal electrode 9 protrudes to the left-side end part and a ceramic dielectric layer 6 in which an internal electrode 10 is put aside to the right-side end part, are laminated; a laminated body 15 is formed. The laminated body 15 is ground up to parts A, B by using a grinding machine, a sandblast or the like; all the internal electrodes 7, 8, 9, 10 are taken out and used as electrodes; outer electrodes 13, 14 are formed. Thereby, the rated voltage and the capacity of the title capacitor can be changed, the thickness of the laminated body can be reduced, the rated voltage is reduced and the electrostatic capacity of the title capacitor can be changed largely.



LEGAL STATUS

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[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	2972000
[Date of registration]	27.08.1999
[Number of appeal against examiner's decision of	

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] In the stacked type ceramic condenser which carries out the laminating of the dielectric layer of two or more layers which has the internal electrode of two or more layers Before carrying out the laminating of two or more internal electrodes with which distance differs from capacity regularly and forming an external electrode, a grinding machine, sandblasting, etc. are used. By deleting the ceramic and internal electrode of an end face of the direction of a right angle of straight side [of a stacked type ceramic condenser] [of an internal electrode] The manufacture approach of the stacked type ceramic condenser characterized by carrying out adjustment change of rated voltage and the capacity by changing the effective number of layers which forms an internal electrode in an end face and forms the distance and capacity of a bond and a dielectric layer in a drawing external electrode.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the manufacture approach of a stacked type ceramic condenser.
[0002]
[Description of the Prior Art] Conventionally, this kind of stacked type ceramic condenser forms membranes by uniform thickness, and the same pattern is not made as for adjustment of rated voltage to for example, a carrier film etc. by it, in order to put, printing and. Moreover, since capacity would be decided once it piles up the number of predetermined sheets also about capacity, there was a fault that capacity could not be adjusted.
[0003]
[Problem(s) to be Solved by the Invention] This invention forms uniform thickness on a carrier film in order to remove these faults. On a carrier film, after carrying out printing membrane formation, that from which an internal electrode pattern differs is printed. The part from which the internal electrode pattern was taken out by the chip front face before accumulating regularly the internal electrode with which the patterns differ and forming an external electrode by deleting a ceramic and an internal electrode using a grinding machine, sandblasting, etc. It aims at offering the stacked type ceramic condenser which adjusts rated voltage and capacity.
[0004]
[Means for Solving the Problem] In the stacked type ceramic condenser with which this invention carries out the laminating of the dielectric layer of two or more layers which has the internal electrode of two or more layers Before carrying out the laminating of two or more internal electrodes with which distance differs from capacity regularly and forming an external electrode, a grinding machine, sandblasting, etc. are used. By deleting the ceramic and internal electrode of an end face of the direction of a right angle of straight side [of a stacked type ceramic condenser] [of an internal electrode] It is the manufacture approach of the stacked type ceramic condenser characterized by carrying out adjustment change of rated voltage and the capacity by changing the effective number of layers which forms an internal electrode in an end face and forms the distance and capacity of a bond dielectric layer in a drawing external electrode.
[0005]
[Function] By deleting a ceramic and an internal electrode from the part from which some internal electrodes inserted into the interior of a layered product are taken out by the chip front face using a grinding machine, sandblasting, etc., rated voltage and capacity can be changed, thickness of a layered product is made small, rated voltage also becomes small, and this invention can offer the stacked type ceramic condenser which can double [more than] electrostatic capacity, before forming an external electrode.
[0006]
[Example] An example is explained below. Drawing 1 is the top view of ceramic dielectric layer A3 of width of face W out of which the internal electrode A7 came to the right side edge section. Drawing 2 is the top view of ceramic dielectric layer B4 of the width of face W which the internal electrode B8 depended on the left side edge section. Drawing 3 , the top view of the ceramic dielectric layer C5 of width of face W out of which ********** C9 came to the left side edge section. Drawing 4 is the top view of the ceramic dielectric layer D6 of the width of face W which the internal electrode D10 depended on the right side edge section. Drawing 5 is the perspective view which carried out the laminating of the ceramic dielectric layer of ceramic dielectric A3 of drawing 1 , drawing 2 , drawing 4 , drawing 3 , drawing 4 , drawing 2 , and drawing 1 , ceramic dielectric B4, a ceramic dielectric C5, and a ceramic dielectric D6, and formed the

layered product 15. (a) of drawing 6 is the sectional view of the stacked [redacted] ceramic condenser A1 which formed the external electrodes A111 and A212 in the layered product 15 which has the internal electrodes A7, B8, C9, and D10 of drawing 5 . (b) of drawing 6 is the sectional view of stacked type ceramic condenser B-2 which carries out grinding to A and B, has internal electrodes A7, B8, C9, and D10, and gave the external electrodes B113 and B214. Drawing 7 is the perspective view of the stacked type ceramic condenser A1 of drawing 6 . Drawing 8 is the perspective view of stacked type ceramic condenser B-2 of drawing 7 . When stacked type ceramic condenser A1 and B-2 as shown in drawing 7 and drawing 8 are manufactured, The ceramic dielectric layer shown in drawing 1 , drawing 2 , drawing 3 , and drawing 4 , respectively For example, the ceramic dielectric layer A3-> ceramic dielectric layer B4-> ceramic dielectric layer D6 -> ceramic dielectric layer C5 -> A laminating is regularly carried out like ceramic dielectric layer D6 -> ceramic dielectric layer B4-> ceramic dielectric layer A3. If it passes through a debinder baking process, the layered product 15 of the width of face W as shown in drawing 5 , and thickness T will be obtained. The condition of the internal electrode of the internal electrode A7 currently formed in the interior of a layered product 15, an internal electrode B8, an internal electrode C9, and an internal electrode D10 has the following descriptions. An internal electrode A7 is made to form on the one side front face of ceramic dielectric layer A3 of drawing 1 , an internal electrode B8 is formed on the one side front face of ceramic dielectric layer B4 of drawing 2 , and this internal electrode does not have a fetch electrode. An internal electrode C9 is made to form on the one side front face of the ceramic dielectric layer C5 of drawing 3 . An internal electrode D10 is formed on the one side front face of the ceramic dielectric layer D6 of drawing 4 , and this internal electrode does not have a fetch electrode. These ceramic dielectric layers For example, when a laminating is regularly carried out like ceramic dielectric layer A3-> ceramic dielectric layer B4-> ceramic dielectric layer D6 -> ceramic dielectric layer C5 -> ceramic dielectric layer D6 -> ceramic dielectric layer B4-> ceramic dielectric layer A3, Each ceramic dielectric layer so that the dimension W of a layered product 15 comes to be in agreement with the cross direction W of ceramic dielectric layer A3 and B4, C5, and D6 as shown in drawing 5 R> 5, and the dimension T of a layered product 15 may become smaller than a dimension W for example Ceramic dielectric layer A3-> ceramic dielectric layer B4-> ceramic dielectric layer D6 -> ceramic dielectric layer C5 -> the number of laminatings of ceramic dielectric layer D6 -> ceramic dielectric layer B4-> ceramic dielectric layer A3 is chosen. Thus, when a laminating is carried out, internal electrodes A7, B8, C9, and D10 are horizontally suitable within the layered product 15 of drawing 5 . To the layered product 15 of drawing 5 , as shown in drawing 7 , the external electrodes A111 and A212 are formed. It is (a) of drawing 6 R> 6 which made the layered product of drawing 7 the crosswise cross section. As it becomes as shown in (b) of drawing 6 when grinding of the ceramic is carried out and it is removed with finishing machines, such as a grinding machine, to the line of A and B of (a) of drawing 6 , and shown in (b) of drawing 6 , the external electrodes B113 and B214 are altogether formed by using internal electrodes A7, B8, C9, and D10 as a drawing electrode. It forms A212. for example, the inside of the layered product 15 of drawing 5 -- ceramic dielectric layer B4 and the electrode of D6 -- each -- the external electrode A111 -- If a ceramic and an internal electrode are deleted and it forms like the external electrodes B113 and B214 of drawing 8 with a grinding machine, sandblasting, etc. until it is taken out by the front face As shown in drawing 8 , the dielectric layer of the layered product of drawing 7 serves as one third of thickness, and it becomes possible to change rated voltage into 1/3WV, and to change electrostatic capacity about 2.5 times. Furthermore, it is also possible to diversify the rated voltage which can choose the pattern formed in a ceramic dielectric by increasing from these four patterns, and electrostatic capacity. Moreover, although the layered product of this drawing 5 showed the example which is carrying out the laminating horizontally, creation in a perpendicular direction is also possible. When the green sheet of 20-micrometer thickness was actually used for the prototype using the ingredient of Pb[(MgW) 0.2 (NiNb) 0.4Ti0.4] O3 system, the layered product was made like drawing 7 and drawing 8 and the electrical property was measured, the result as shown in a table 1 was obtained.

[A table 1]

図番	定格電圧	研削機やｻﾝﾄﾞﾌﾞﾗｽﾄ等処理	静電容量（C値）	破壊電圧（B.D.V）
図7	75V	無	0.4μF	1.0KV
図8	25V	有	1 μF	300V

[0007]
[Effect of the Invention] As stated above, before according to this invention diversifying inside the pattern which carries out a laminating and forming an external electrode in it, offer of a stacked type ceramic condenser with the advantage that rated voltage and electrostatic capacity can be changed was attained by deleting the external electrode drawing side by the grinding machine, sandblasting, etc.

[Translation done.]

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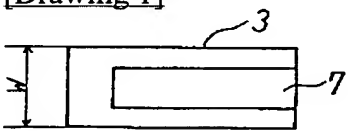
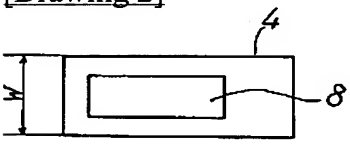
DRAWINGS

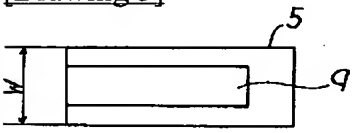
[Drawing 1]



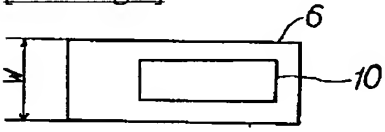
[Drawing 2]



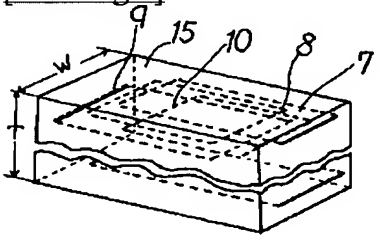
[Drawing 3]



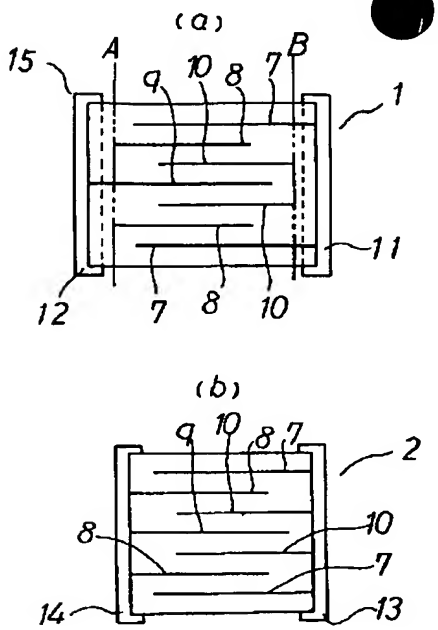
[Drawing 4]



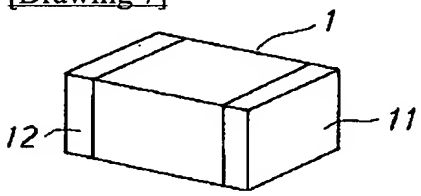
[Drawing 5]



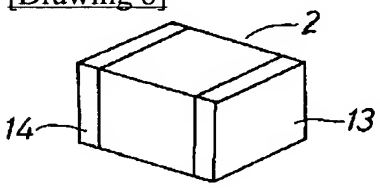
[Drawing 6]



[Drawing 7]



[Drawing 8]



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